Claims

What is claimed is:

1. A method of testing at least one semiconductor chip using an external tester, comprising:

reading a stored bit from a memory array on said at least one semiconductor chip;

preventing said stored bit from being output from said at least one semiconductor chip;

allowing said at least one semiconductor chip to receive an expected bit from said tester; and

comparing said stored bit and said expected bit.

2. The method in claim 1, wherein

said act of reading comprises reading a plurality of stored bits from a respective plurality of semiconductor chips;

said act of preventing comprises preventing said plurality of stored bits from being output from said plurality of semiconductor chips; and

said act of allowing comprises allowing said plurality of semiconductor chips to simultaneously receive an expected bit from said tester.

3. The method in claim 2, further comprising saving an address corresponding to said stored bit in an on-chip register in response to said stored bit failing to match said expected bit.

4. The method in claim 3, wherein said comparing act further comprises comparing said stored bit and said expected bit, and wherein a failure of said stored bit to match said expected bit results in:

replacing a memory cell associated with said address with a redundant memory cell, and

replacing at least one other memory cell having an adjacent address with at least one other redundant memory cell.

5. The method in claim 4, wherein said act of comparing said stored bit and said expected bit comprises comparing said stored bit and said expected bit on said at least one semiconductor chip.

6. The method in claim 5, wherein said step of preventing said stored bit from being output from said at least one semiconductor chip comprises tri-stating an output circuit of said at least one semiconductor chip.

7. The method in claim 6, wherein said act of tri-stating an output circuit of said at least one semiconductor chip comprises isolating said output circuit from a generally constant positive voltage source and from ground.

8. The method in claim 7, further comprising:

writing a test bit from said tester to said plurality of semiconductor chips before said act of reading a stored bit from a memory array; and

saving said test bit on said plurality of semiconductor chips as said stored bit.

9. The method in claim 8, further comprising rewriting said test bit from said tester to said plurality of semiconductor chips after said act of replacing a memory cell.

10. A method of dealing with a failed memory cell on a semiconductor die, comprising:

providing a register on said semiconductor die, wherein said register is configured to avoid storing multiple addresses at any time; and

storing a first memory address in said register, wherein said first memory address corresponds to a first failed memory cell.

11. The method in claim 10, further comprising storing a second memory address in said register in place of said first memory address in response to detecting a second failed memory cell, wherein said second memory address corresponds to said second failed memory cell.

12. The method in claim 11, wherein said act of storing a first memory address comprises:

storing a first column address of said first failed memory cell; and

excluding from storage a first row address of said first failed memory cell.

13. The method in claim 12, wherein said act of providing a register comprises providing a register configured to store:

data indicating a presence of at least one failed memory cell; and

at most one memory address.

14. The method in claim 13, wherein said act of providing a register comprises providing a register configured to store a single bit indicating the presence of at least one failed memory cell.

15. The method in claim 14, further comprising rerouting a signal relevant to a column address stored in said register from a first column of memory cells to a redundant column of memory cells.

16. The method in claim 15, further comprising testing said semiconductor die after said act of rerouting.

17. The method in claim 16, further comprising testing said semiconductor die before said act of rerouting, wherein said act of testing said semiconductor die before said act of rerouting is configured to identify said first failed memory cell.

18. A method of repairing a region of memory on a semiconductor chip

replacing at least one defective memory cell with at least one redundant memory cell; and

replacing at least one non-defective memory cell with at least one additional redundant memory cell, wherein said at least one non-defective memory cell is associated with said at least one defective memory cell;

wherein said acts of replacing at least one defective memory cell and replacing at least one non-defective memory cell use all redundant memory cells designated for repair of said region of memory on said semiconductor chip.

19. The method in claim 18, wherein said act of replacing at least one non-defective memory cell comprises replacing at least one non-defective memory cell sharing a common conductive line with said at least one defective memory cell.

20. The method in claim 19, wherein said act of replacing at least one non-defective memory cell comprises replacing at least one non-defective memory cell sharing a common column address with said at least one defective memory cell.

21. The method in claim 20, further comprising providing an indication of an existing defective memory cell, wherein said act of providing an indication comprises storing a particular value in a register on said semiconductor chip.

22. The method in claim 21, wherein said register is configured to store said common column address; and wherein said common column address and said value fill said register.

23. The method in claim 22, wherein said act of storing a particular value is in response to testing comprising on-chip comparison of data read from said region of memory and expected data transmitted from an external testing device, wherein said data read from said region of memory and said expected data do not match.

24. A process for supplemental testing of a memory chip, comprising:

determining whether said memory chip has been repaired;

performing a first test in response to said memory chip having been repaired; and

foregoing said first test in response to said memory chip not having been repaired.

25. The process in claim 24, further comprising performing a second test on said memory chip, wherein failing said second test results in repairing an address on said memory chip in response to said address not having been previously repaired.

26. The process in claim 25, wherein said process further comprises:

performing said first test on said memory chip;

repairing said memory chip in response to failing said first test; and

at least temporarily refraining from repairing said memory chip in response to passing said first test.

27. The process in claim 26, further comprising:

during said first test, storing in a register all failed addresses resulting from said first test;

storing a fail flag in said register resulting from the existence of a failed address; and

by the end of said first test, storing in said register only the latest failed address of all failed addresses resulting from said first test.

28. The process in claim 27, wherein said first test is configured for:

replacing at most one column of memory cells with a redundant column of memory cells; and

replacing at least one column of memory cells with a redundant column of memory cells in response to detecting at least one defective cell during a first cycle of said first test.

29. A method of handling an address associated with a memory cell that has failed a test, comprising:

storing said address in a register in response to said memory cell being a non-redundant memory cell; and

clearing any other address from said register in response to said storing act.

30. The method in claim 29, further comprising refraining from storing said address in response to said memory cell being a redundant memory cell.

31. The method in claim 30, further comprising storing a fail flag in said register regardless of whether said memory cell is a redundant or non-redundant memory cell.

32. The method in claim 31, further comprising clearing said address and said fail flag from said register before initiating a subsequent test.

33. A method of processing a semiconductor die having memory cells including main memory cells and redundant memory cells, said method comprising:

checking said semiconductor die for at least one defective memory cell;

storing at most one address at a time in a register on said die, wherein said address corresponds to a column address of a defective main memory cell identified during said act of checking; and

replacing with redundant memory cells all main memory cells having a column address matching one column address stored in said register.

34. The method in claim 33, wherein said act of checking comprises checking said semiconductor die while said semiconductor die is in a singulation state selected from a group consisting of said die being part of a wafer, said die being integral with at least one other die yet separate from a wafer, and said die being completely singulated from all other die.

35. The method in claim 33, wherein said act of checking comprises checking said semiconductor die while said semiconductor die exhibits a packaging state ranging from a bare die to part of a fully packaged chip.

36. The method in claim 33, wherein said act of checking comprises checking said semiconductor die using a selection comprising an AMBYX device and a TERADYNE device.

37. The method in claim 33, wherein said act of checking comprises performing a process on said die, wherein said process is selected from a group consisting of a test, a probe, a cold burn-in, and a non cold burn-in process.

38. The method in claim 33, wherein said act of replacing comprises replacing with redundant memory cells all main memory cells having a column address matching a last column address stored in said register.

39. The method in claim 33, wherein said act of replacing comprises replacing with redundant memory cells all main memory cells having a column address matching a first column address stored in said register.

40. The method in claim 33, wherein said act of checking comprises transferring data to said semiconductor die using a mode selected from a group consisting of a compression mode and a non-compression mode.

41. The method in claim 33, wherein said act of checking comprises checking a die exhibiting a latency selected from a group consisting of a latency of 1 and a latency of 2.

42. A circuit for a semiconductor chip including a memory array and an address latch, wherein said chip is configured to electrically communicate with a terminal of a tester, said circuit comprising:

a comparator on said semiconductor ship coupled to said memory array and to said terminal of said tester, wherein said comparator is configured to receive a first data value from said memory array and a second data value from said terminal and further configured to transmit a signal based upon a lack of identity between said first and second data values.

43. The circuit in claim 42, further comprising a register coupled to said address latch and to said comparator, wherein said first data value is associated with an address transmitted by said address latch, and wherein said register is configured to store said address in response to receiving said signal from said comparator.

44. The circuit in claim 43, wherein said register is configured to store less than two addresses at one time.

45. The circuit in claim 44, wherein said register is configured to preferably store a later address corresponding to a later transmission of said signal over a prior address corresponding to a prior transmission of said signal.

46. The circuit in claim 45, wherein said register is also configured to store at least one bit indicating a reception of said signal.

47. The circuit in claim 45, further comprising an output circuit comprising:

an inverter coupled to said memory array;

a first transistor electrically interposed between said inverter and a positive voltage source and configured to turn off during a test mode for said semiconductor chip; and

a second transistor electrically interposed between said inverter and ground and configured to turn off during said test mode.

48. The circuit in claim 47, further comprising a buffer electrically interposed between said terminal and said comparator.

49. The circuit in claim 48, wherein said comparator comprises an exclusive nor gate.

50. A computer system, comprising:

microprocessor logic;

memory coupled to said microprocessor logic;

an output circuit coupled to said memory, located on a common chip with said memory, and configured to inactivate during a test read mode;

a plurality of redundant memory cells on said chip;

a register on said chip sized to store a fail flag bit and a single column address; and

comparison circuitry on said chip configured to receive a first bit from an external tester and a second bit from a selection of a memory cell from said memory and a redundant memory cell from said plurality of redundant memory cells, said comparison circuitry further configured to signal said register in response to a failure of said first and second bit to match.

51. The system in claim 50, further comprising an anti-fuse bank configured to divert to a redundant memory cell an electrical transmission for any memory cell in said memory that shares a column address with a defective cell.

52. The system in claim 51, wherein said memory comprises a selection from a group consisting of nonvolatile, static, and dynamic memory.

53. The system in claim 52, wherein said memory comprises a selection from a group consisting of a discrete memory device, embedded memory in a chip with logic, and one of a plurality of components in a system on a chip.